CAREER INFORMATION AND RECRUITMENT PORTAL

PROJECT REPORT

submitted by

**JINCY P JANARDHANAN** (IEAREIT017)

**ALEENA SUNNY** (IEAREIT006)

**ALKA BHAGAVALDAS** (IEAREIT007)

**AMEENA SHIRIN** (IEAREIT009)

to

the University of Calicut

in partial fulfilment of the requirements for the award of the Degree

of

**Bachelor of Technology**

in

Information Technology



Department of Information Technology

Institute of Engineering and Technology, University of Calicut, Thenjipalam

Kerala

July 18, 2020

DECLARATION

We undersigned hereby declare that the project report **Career Information and Recruitment Portal**, submitted for partial fulfilment of the requirements for the award of degree of Bachelor of Technology of the University of Calicut, Kerala is a bonafide work done by us under supervision of **Ms. Sruthimol M P**. This submission represents our ideas in our own words and where ideas or words of others have been included, we have adequately and accurately cited and referenced the original sources. We also declare that we have adhered to ethics of academic honesty and integrity and have not misrepresented or fabricated any data or idea or fact or source in our submission. We understand that any violation of the above will be a cause for disciplinary action by the institute and/or the University and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been obtained. This report has not been previously formed the basis for the award of any degree, diploma or similar title of any other University.

**Place:** Thenjipalam

**Date:** July 18, 2020

Jincy P Janardhanan

Aleena Sunny

Alka Bhagavaldas

Ameena Shirin

DEPARTMENT OF INFORMATION TECHNOLOGY  
INSTITUTE OF ENGINEERING AND TECHNOLOGY UNIVERSITY OF CALICUT, THENJIPALAM



CERTIFICATE

This is to certify that the report entitled **"CAREER INFORMATION AND RECRUITMENT PORTAL",** submitted by **Jincy P Janardhanan, Aleena Sunny, Alka Bhagavaldas, Ameena Shirin** to the **UNIVERSITY OF CALICUT** in partial fulfilment of the requirements for the award of the degree of Bachelor of Technology in Information Technology is a bonafide record of the project presented by them under our guidance and supervision. This report in any form has not been submitted to any other University or Institute for any purpose.

|  |  |
| --- | --- |
| **Ms. Anu Manohar**  Assistant Professor  Department of IT  (Coordinator) | **Ms. Sruthimol M P**  Lecturer  Department of IT  (Coordinator & Guide) |

ACKNOWLEDGEMENT

We would like to express our warmest gratitude to all the people who had been a great help, support and motivation throughout this project. Prima facie, we would like to thank the Almighty for giving us the wisdom and grace for the successful completion of our project. Forever we owe our deepest gratitude to our guide and coordinator, **Ms. Sruthimol M P**, Lecturer, Department of Information Technology, for her expert guidance, co-operation and immense encouragement in pursuing this project. With a profound sense of gratitude, we would like to express our heartfelt thanks to our coordinator, **Ms. Anu Manohar**,Assistant Professor, Department of Information Technology for her earnest co-operation, support and constant inspiration. We extend our sincere gratitude to all the teachers of the Department of IT and to all our friends for their help and support.

Jincy P Janardhanan

Aleena Sunny

Alka Bhagavaldas

Ameena Shirin

ABSTRACT

Contents

[List of Figures viii](#_Toc46003693)

[List of Tables ix](#_Toc46003694)

[Abbreviations x](#_Toc46003695)

[Chapter 1 Introduction 1](#_Toc46003696)

[1.1 Problem Statement 1](#_Toc46003697)

[1.2 Motivation and Objective 1](#_Toc46003698)

[Chapter 2 Literature Review 4](#_Toc46003699)

[2.1 Existing Methodologies 4](#_Toc46003700)

[Chapter 3 Proposed System and Feasibility Study 7](#_Toc46003701)

[3.1 Proposed Solution 7](#_Toc46003702)

[3.2 Technical Feasibility 7](#_Toc46003703)

[3.3 Operational Feasibility 7](#_Toc46003704)

[3.4 Economic Feasibility 7](#_Toc46003705)

[3.5 Schedule Feasibility 8](#_Toc46003706)

[Chapter 4 Requirements Gathering and Analysis 10](#_Toc46003707)

[4.1 End User Specification 10](#_Toc46003708)

[4.2 Software Specification 10](#_Toc46003709)

[4.3 Hardware Specification 10](#_Toc46003710)

[4.4 SRS Document 10](#_Toc46003711)

[Chapter 5 System Design 13](#_Toc46003712)

[5.1 System Architecture 13](#_Toc46003713)

[5.2 Interface Design 13](#_Toc46003714)

[5.3 Data Flow Diagrams 13](#_Toc46003715)

[5.4 Data Dictionary 13](#_Toc46003716)

[Chapter 6 Implementation 16](#_Toc46003717)

[6.1 Module Description 16](#_Toc46003718)

List of Figures

List of Tables

Abbreviations

# Introduction

When the first digital computers appeared in the early 1940s,[5] the instructions to make them operate were wired into the machine. Practitioners quickly realized that this design was not flexible and came up with the "stored program architecture" or von Neumann architecture. Thus the division between "hardware" and "software" began with abstraction being used to deal with the complexity of computing.

Programming languages started to appear in the early 1950s[6] and this was also another major step in abstraction. Major languages such as Fortran, ALGOL, PL/I, and COBOL were released in the late 1950 and 1960s to deal with scientific, algorithmic, and business problems respectively. David Parnas introduced the key concept of modularity and information hiding in 1972[7] to help programmers deal with the ever-increasing complexity of software systems.

## Problem Statement

## Motivation and Objective

# Literature Review

## Existing Methodologies

# Proposed System and Feasibility Study

## Proposed Solution

## Technical Feasibility

## Operational Feasibility

## Economic Feasibility

## Schedule Feasibility

# Requirements Gathering and Analysis

## End User Specification

## Software Specification

## Hardware Specification

## SRS Document

# System Design

## System Architecture

## Interface Design

## Data Flow Diagrams

## Data Dictionary

# Implementation

## Module Description